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Transistors FET

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Contents

The FET

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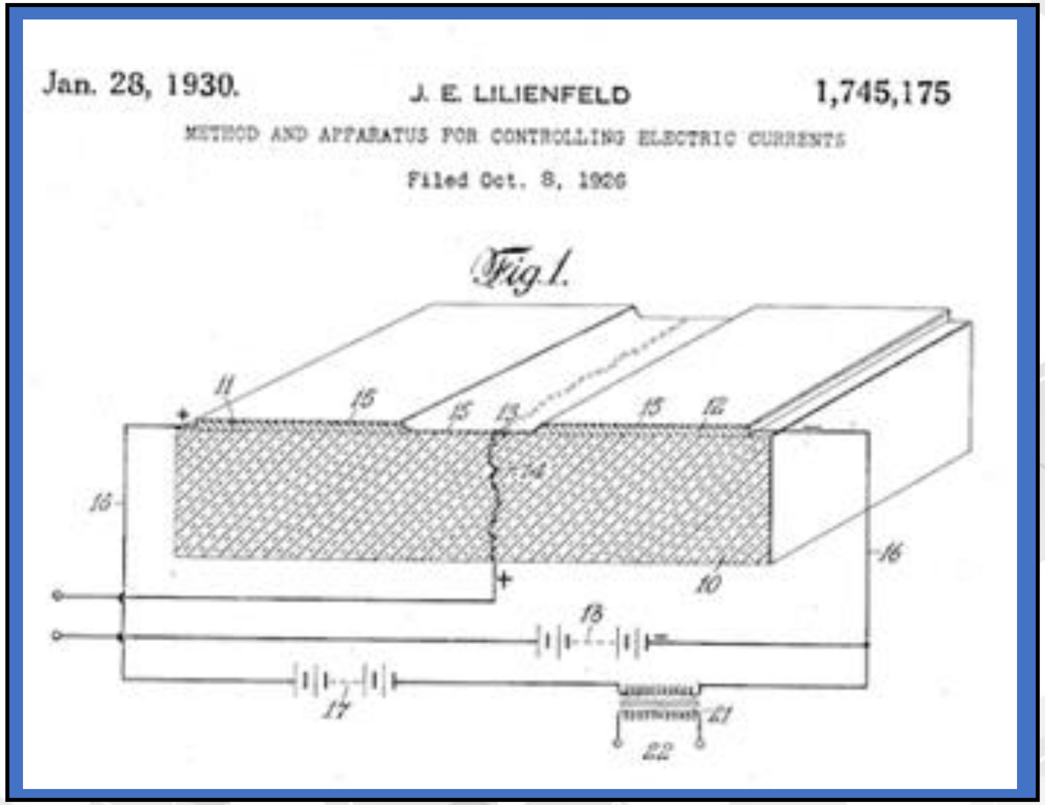
The idea for a field-effect transistor (FET) was first proposed by Julius Lilienthal, a physicist and inventor. In 1930 he was granted a U.S. patent for the device.

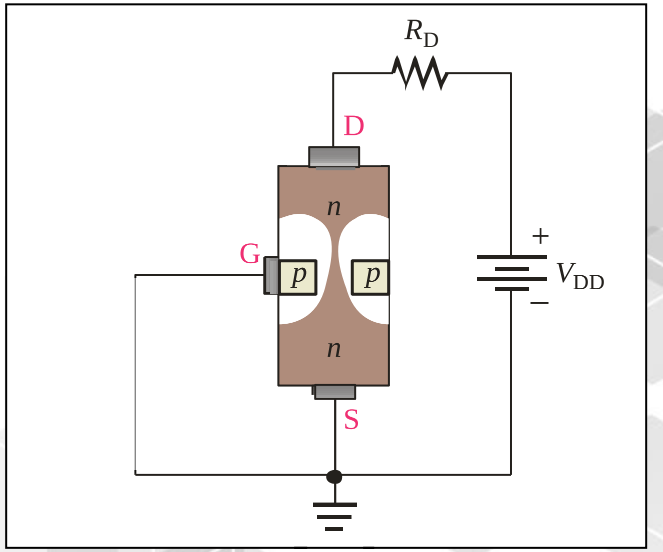
His ideas were later refined and developed into the FET. Materials were not available at the time to build his device. A practical FET was not constructed until the 1950's. Today FETs are the most widely used components in integrated circuits.



The JFET

The JFET (or Junction Field Effect Transistor) is a normally ON device. For the *n*-channel device illustrated, when the drain is positive with respect to the source and there is no gate-source voltage, there is current in the channel.

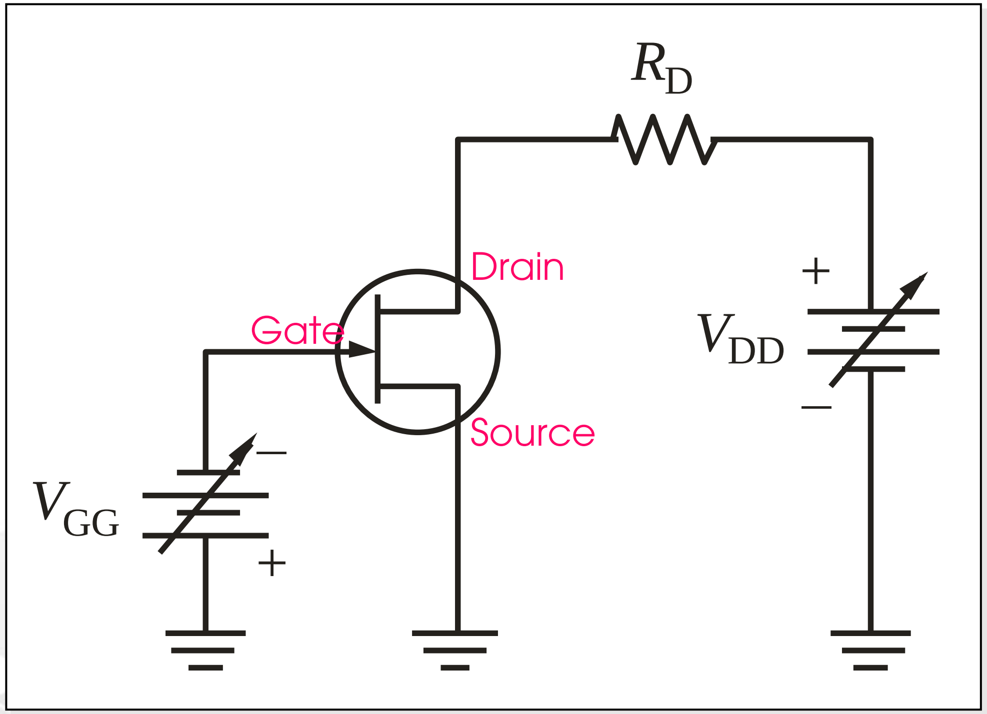
When a negative gate voltage is applied to the FET, the electric field causes the channel to narrow, which in turn causes current to decrease.



The JFET

As in the base of bipolar transistors, there are two types of JFETs: *n*-channel and *p*-channel. The dc voltages are opposite polarities for each type.

The symbol for an *n*-channel JFET is shown, along with the proper polarities of the applied dc voltages. For an *n*-channel device, the gate is always operated with a negative (or zero) voltage with respect to the source.



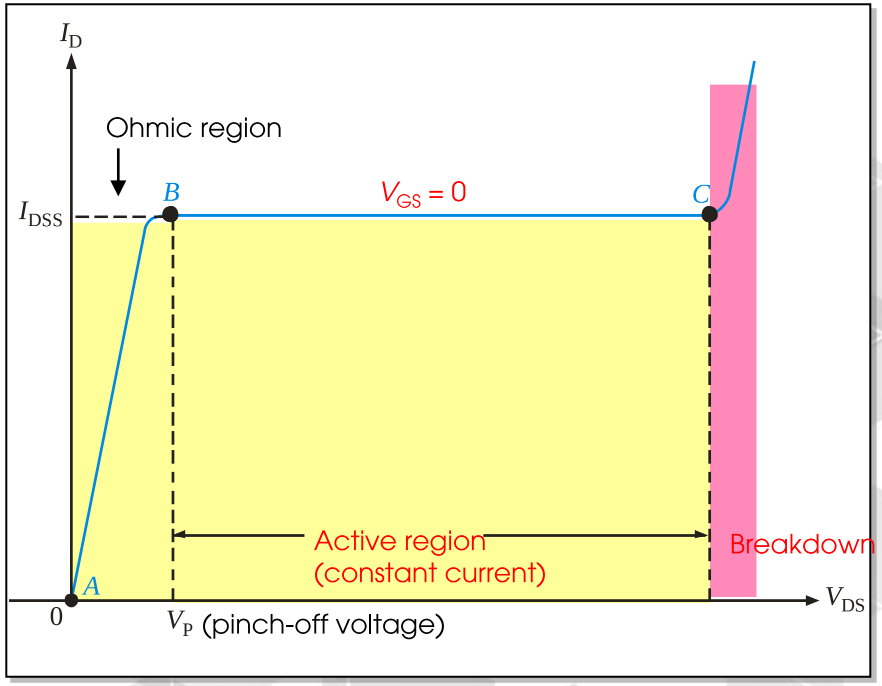
The JFET

There are three regions in the characteristic curve for a JFET as illustrated for the case when $V_{GS} = 0$ V.

Between *A* and *B* is the **Ohmic region**, where current and voltage are related by Ohm's law.

From *B* to *C* is the **active** (or *constant-current*) **region** where current is essentially independent of V_{DS}.

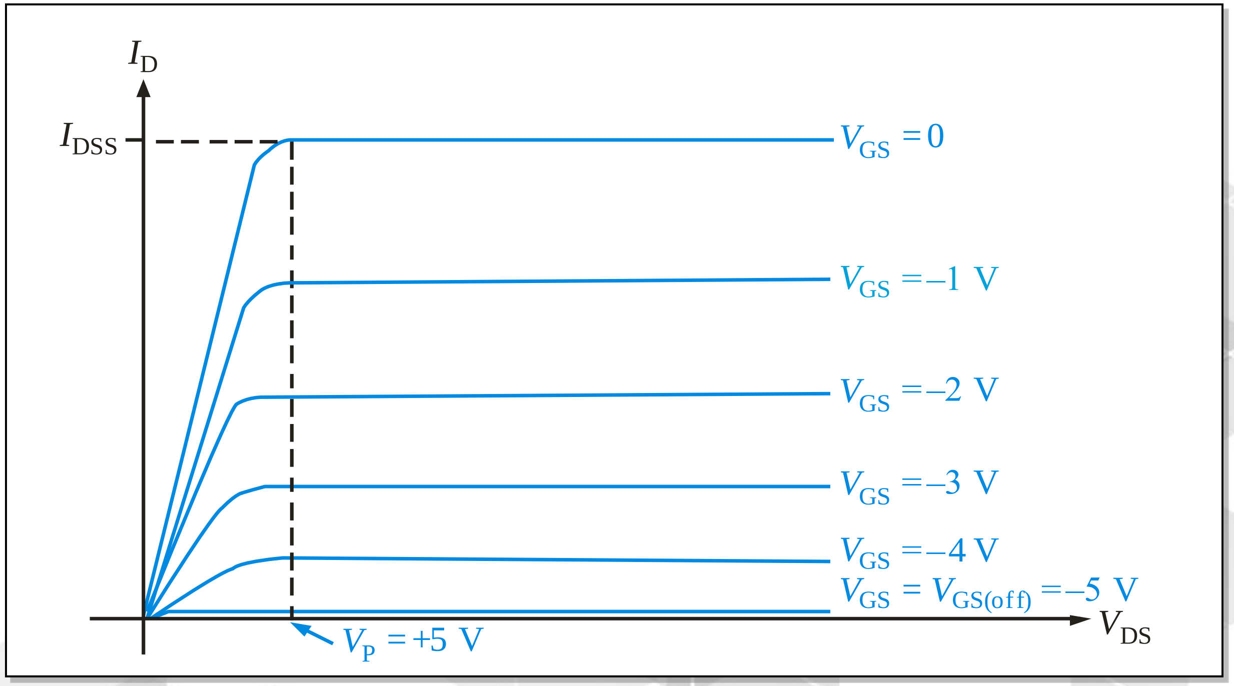
Beyond *C* is the **breakdown region**. Operation here can damage the FET.



The JFET

When V_{GS} is set to different values, the relationship between V_{DS} and I_D develops a family of characteristic curves for the device.

An *n*-channel characteristic is illustrated here. Notice that V_p is positive and has the same magnitude as $V_{GS(off)}$.

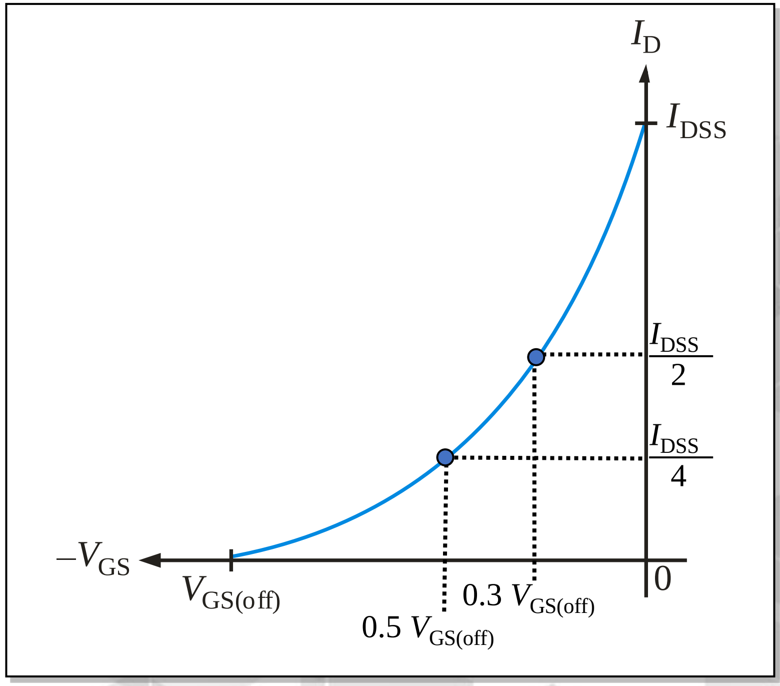


The JFET

A plot of V_{GS} to I_D is called the transfer or transconductance curve. The transfer curve is a is a plot of the output current (I_D) to the input voltage (V_{GS}).

The transfer curve is based on the equation

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$



By substitution, you can find other points on the curve for plotting the universal curve.

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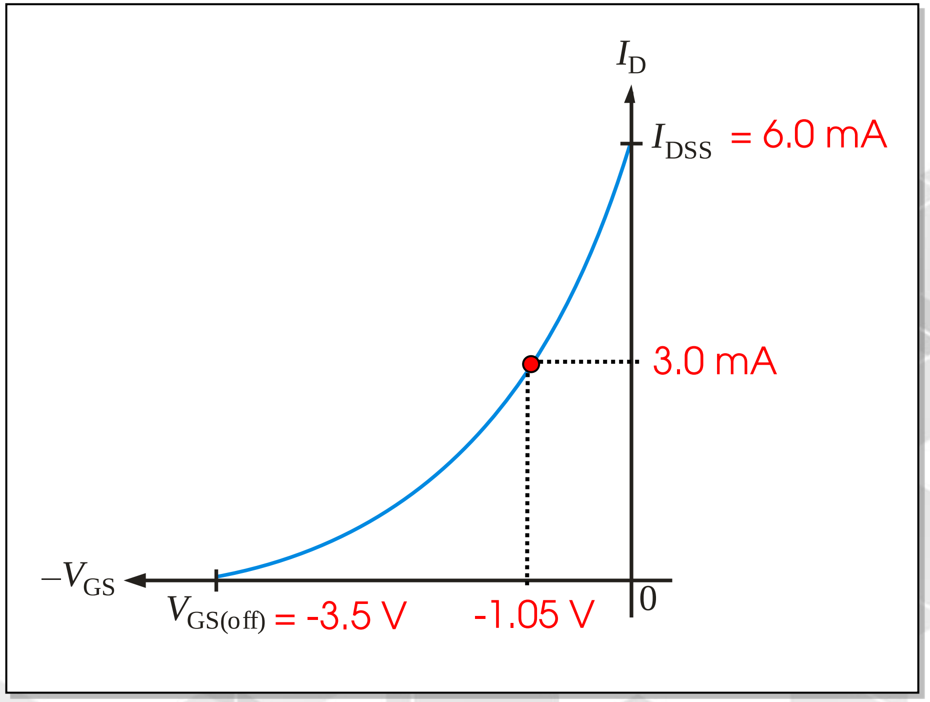
Example:

A certain 2N5458 JFET has $I_{DSS} = 6.0$ mA and $V_{GS(off)} = -3.5$ V.

(a) Show the values of these end points on the transfer curve.

(b) Show the point for the case when $I_D = 3.0$ mA.



Solution:

(b) When $I_D =$ I_{DSS}, $V_{GS} = 0.3 V_{GS(off)}$. Therefore, V_{GS} = -1.05 V

The JFET

The transconductance is the ratio of a change in output current (DI_D) to a change in the input voltage (DV_{GS}).

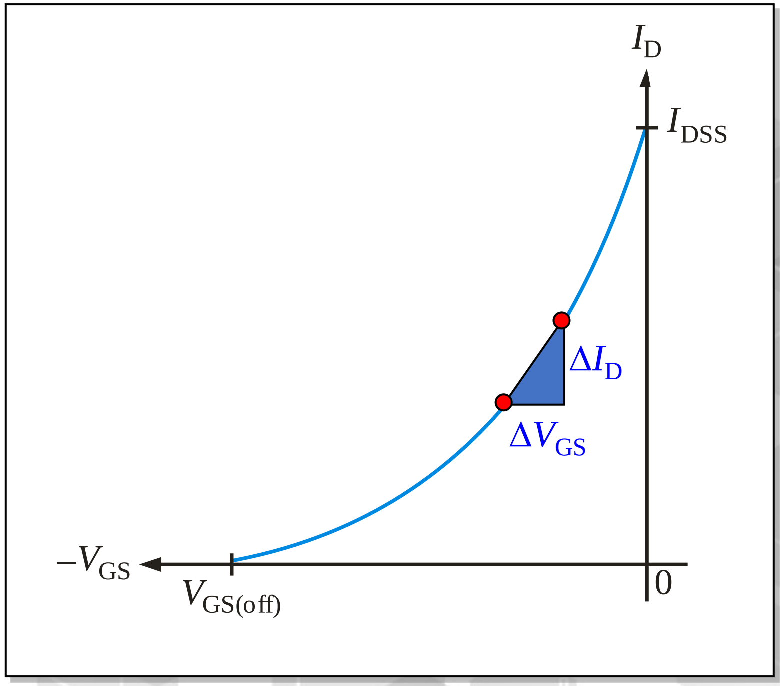
This definition is $g_m = \frac{\Delta I_D}{\Delta V_{GS}}$

The following approximate formula is useful for calculating gm if you know g_{m0}.

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

The value of g_{m0} can be found from

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$$



The JFET

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Because the slope changes at every point along the curve, the transconductance is not constant, but depends on where it is measured.

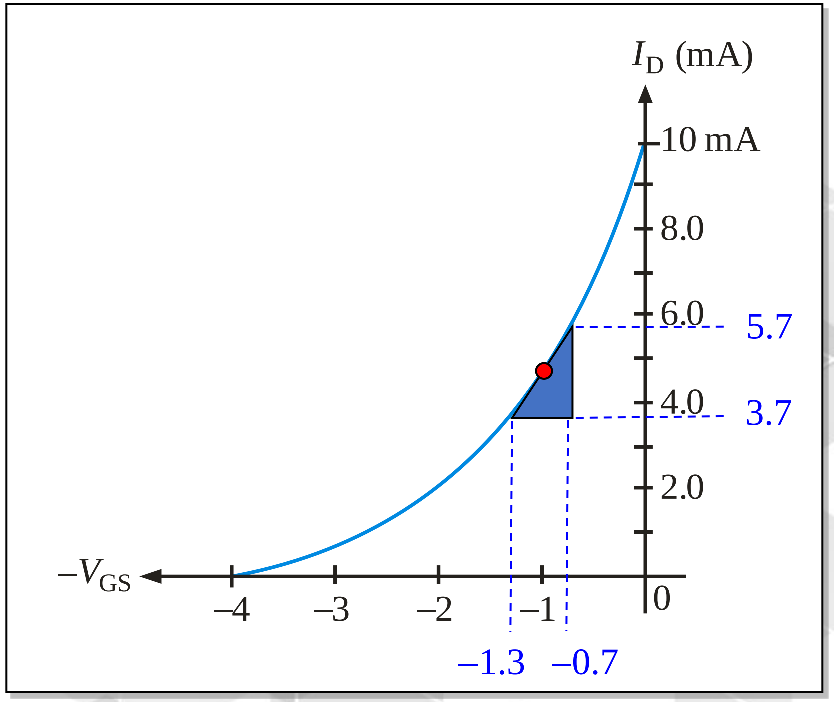
Example:

What is the transconductance for the JFET at the point shown?

Solution:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{5.7\text{ mA} - 3.7\text{ mA}}{-0.7\text{ V} - (-1.3\text{ V})}$$

$$= \frac{2.0\text{ mA}}{0.6\text{ V}} = 3.33\text{ mS}$$



JFET Input Resistance

The input resistance of a JFET is given by: $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$

where I_{GSS} is the current into the reverse biased gate.

JFETs have very high input resistance, but it drops when the temperature increases.

Example:

Compare the input resistance of a 2N5485 at 25 °C and at 100 °C. The specification sheet shows that for V_{GS} = -20 V, I_{GSS} – 1 nA at 25 °C and 0.2 mA at 100 °C.

Solution:

At 25 °C, $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \left|\frac{20\ \text{V}}{1\ \text{nA}}\right| =$ 20 GΩ!

At 100 °C, $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right| = \left|\frac{20\ \text{V}}{0.2\ \mu\text{A}}\right| =$ 100 MΩ

JFET Biasing

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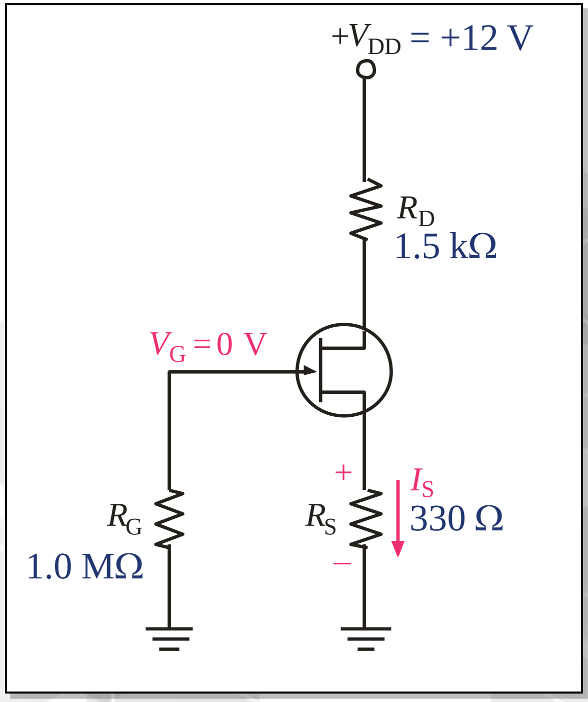
Self-bias is simple and effective, so it is the most common biasing method for JFETs. With self bias, the gate is essentially at 0 V.

An *n*-channel JFET is illustrated. The current in R_S develops the necessary reverse bias that forces the gate to be less than the source.



Example:

Assume the resistors are as shown and the drain current is 3.0 mA. What is V_{GS}?

Solution:

V_G = 0 V; V_S = (3.0 mA)(330 W) = 0.99 V

V_{GS} = 0 – 0.99 V = - 0.99 V

JFET Biasing

You can use the transfer curve to obtain a reasonable value for the source resistor in a self-biased circuit.

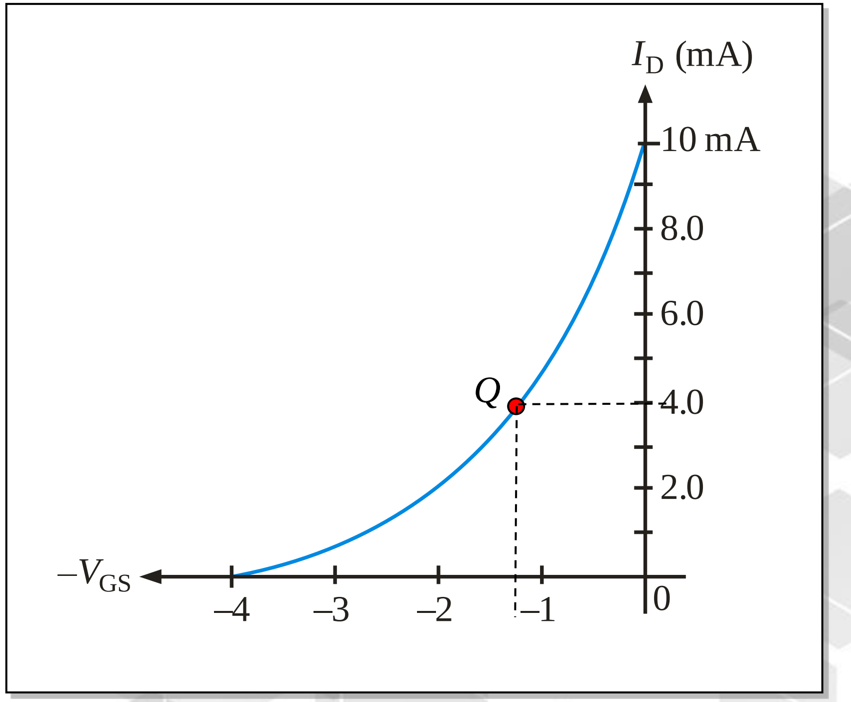
Example:

What value of R_S should you use to set the Q point as shown?

Solution:

The Q point is approximately at I_D = 4.0 mA and V_{GS} = -1.25 V.

$$R_S = \left|\frac{V_{GS}}{I_D}\right| = \frac{1.25\ \text{V}}{3.0\ \text{mA}} = 375\ \Omega$$

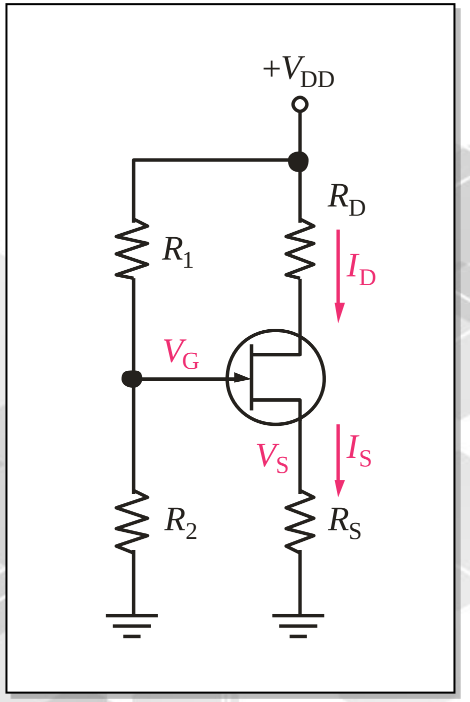


JFET Biasing

Voltage-divider biasing is a combination of a voltage-divider and a source resistor to keep the source more positive than the gate.

V_G is set by the voltage-divider and is independent of V_S. V_S must be larger than V_G in order to maintain the gate at a negative voltage with respect to the source.

Voltage-divider bias helps stabilize the bias for variations between transistors.



JFET Biasing

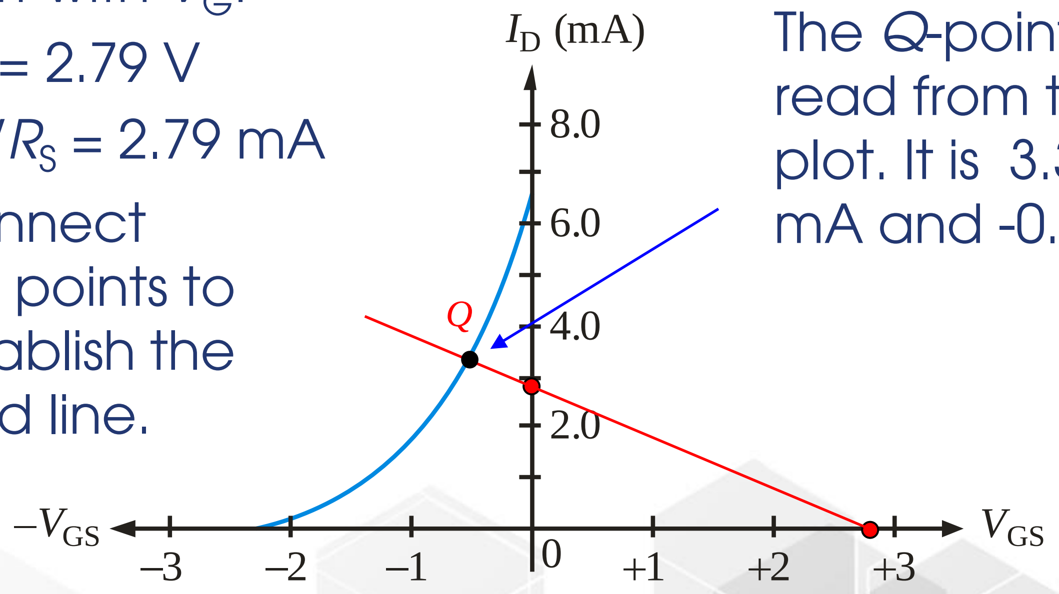
A graphical analysis of voltage-divider biasing is illustrated. A typical transconductance curve for the 2N5485 is shown with I_{DSS} = 6.5 mA and $V_{GS(off)}$ = -2.2 V.

Start with V_G:

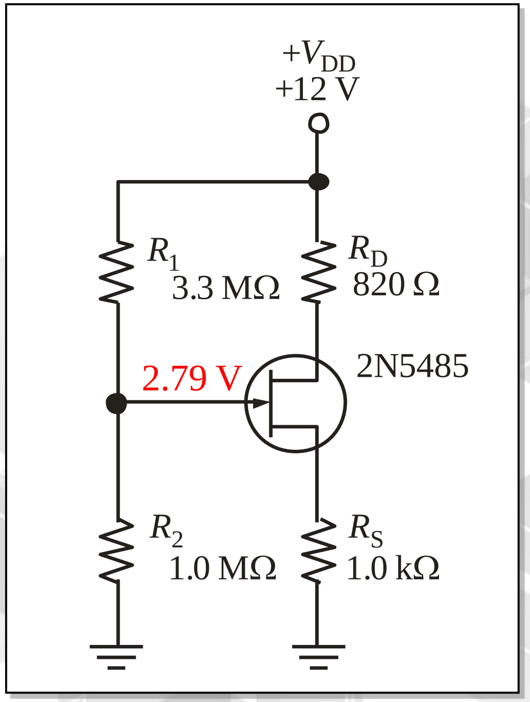
V_G = 2.79 V

V_G/R_S = 2.79 mA

Connect the points to establish the load line.



The Q-point is read from the plot. It is 3.3 mA and -0.7 V.



JFET Biasing

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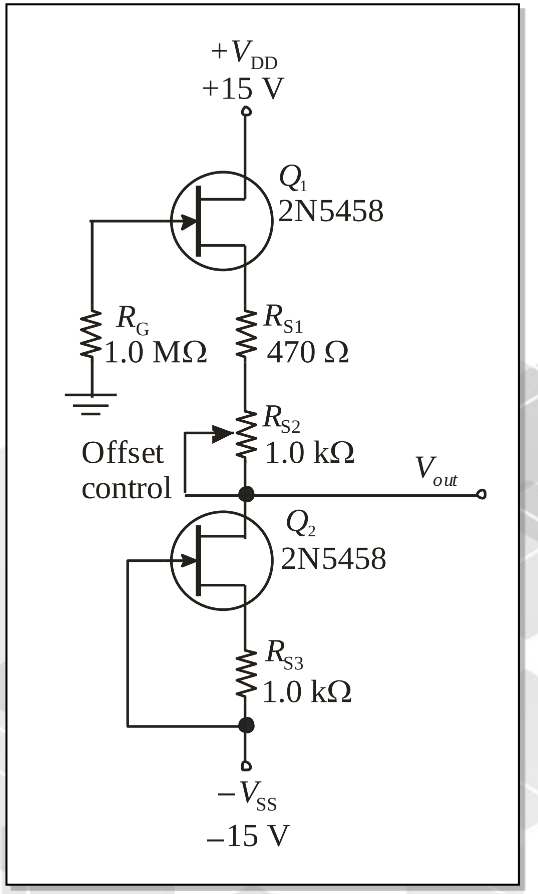
An even more stable form of bias is current-source bias. The current-source can be either a BJT or another FET. With current-source biasing, the drain current is essentially independent of V_{GS}.

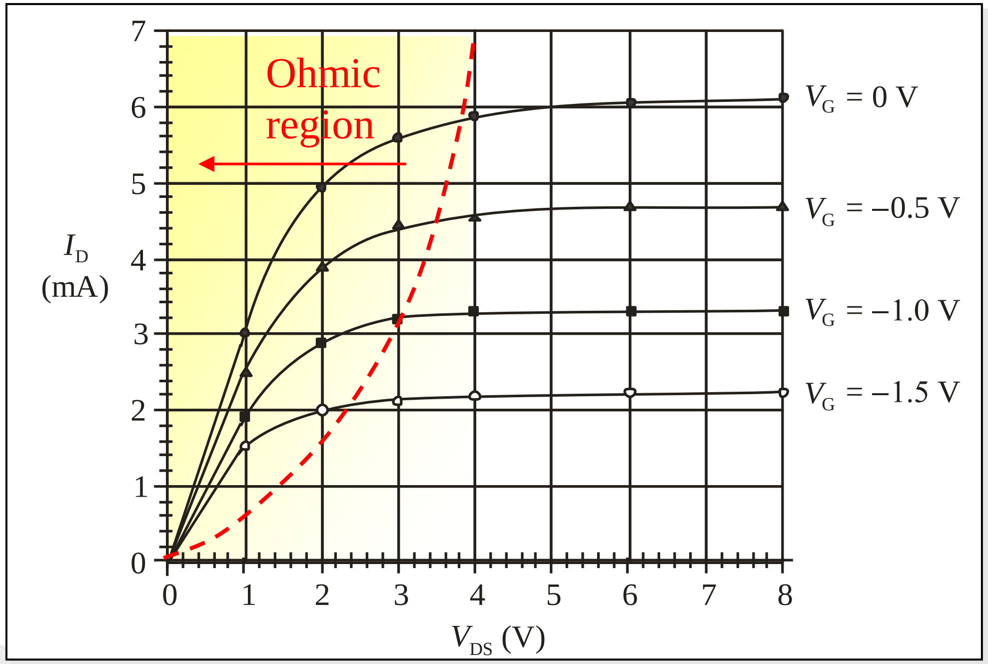
In this circuit Q_2 serves as a current source for Q_1. An advantage to this particular circuit is that the output can be adjusted (using R_{S2}) for 0 V DC.



JFET Ohmic Region

As described before, the ohmic region is between the origin and the active region. A JFET operated in this region can act as a variable resistor.

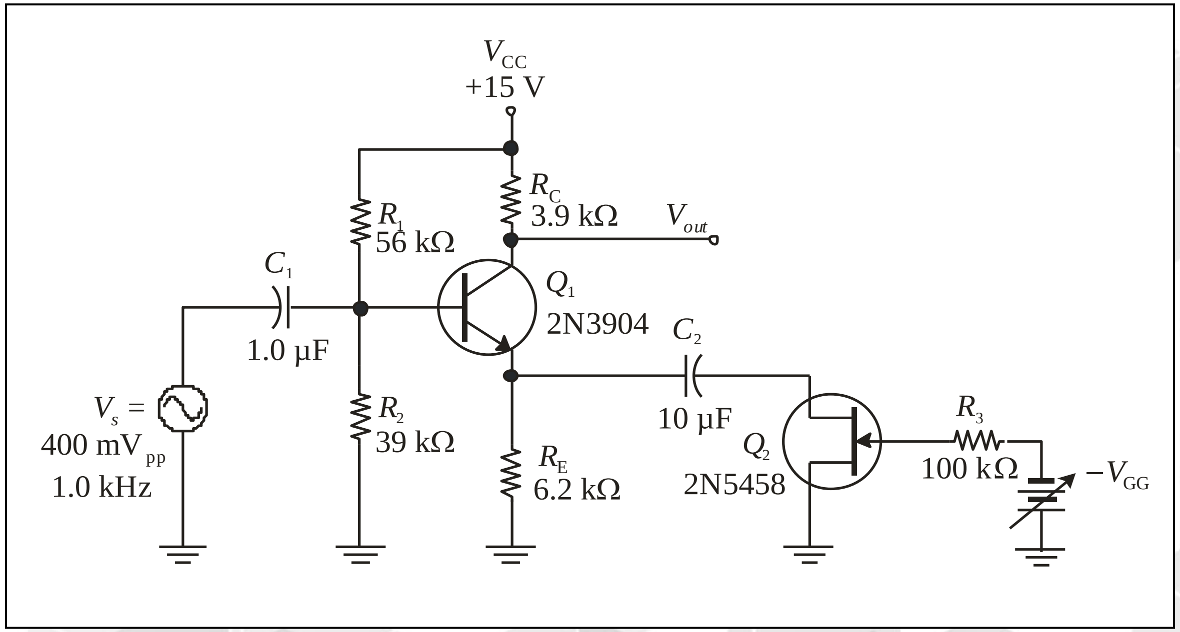
Data from an actual FET is shown. The slopes (which represent conductance) of successive V_{GS} lines are different in the ohmic region. This difference is exploited for use as a voltage controlled resistance.



JFET Ohmic Region

Here is a circuit in which the JFET is used as a variable resistor. Notice that that the drain is connected through a capacitor, which means the JFET's *Q*-point is at the origin.

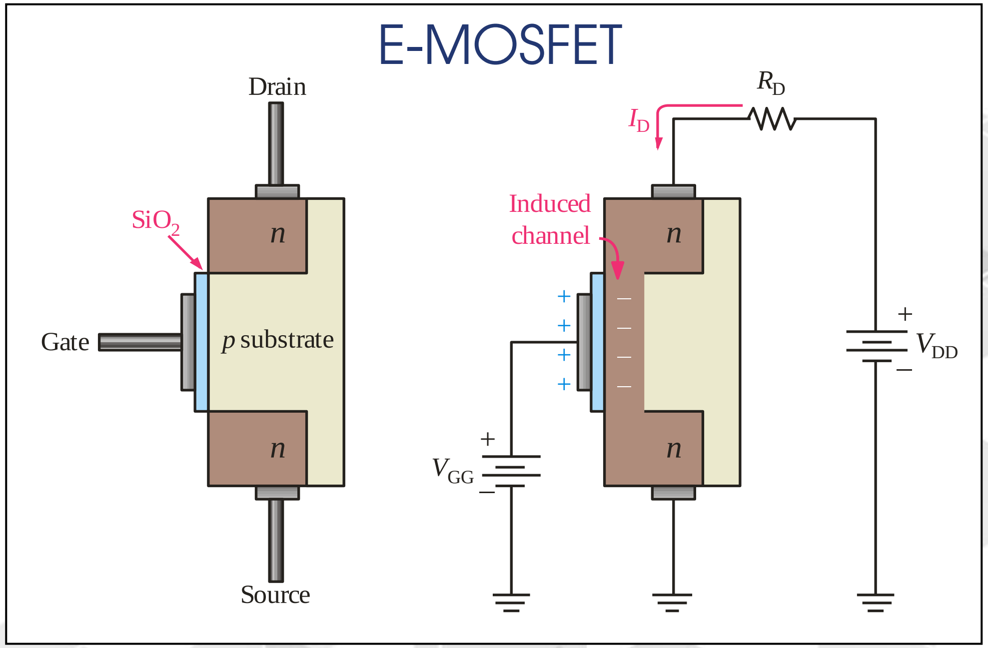
The gain of the BJT depends on the dc voltage setting of V_{GG}.



The MOSFET

The metal oxide semiconductor FET uses an insulated gate to isolate the gate from the channel. Two types are the enhancement mode (E-MOSFET) and the depletion mode (D-MOSFET).

An E-MOSFET has no channel until it is induced by a voltage applied to the gate, so it operates only in enhancement mode. An *n*-channel type is illustrated here; a positive gate voltage induces the channel.

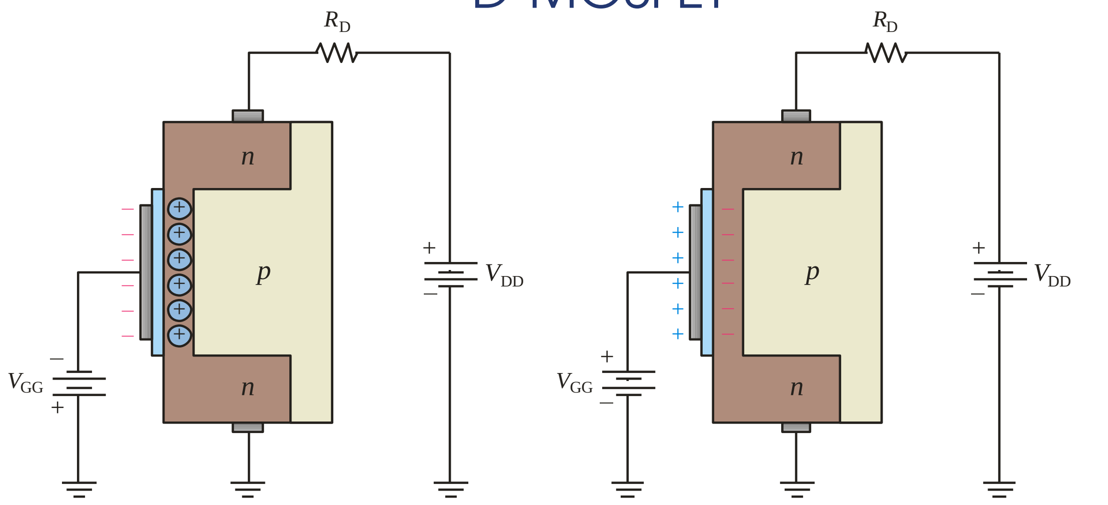


The MOSFET

The D-MOSFET has a channel that can is controlled by the gate voltage. For an *n*-channel type, a negative voltage depletes the channel; and a positive voltage enhances the channel.

A D-MOSFET can operate in either mode, depending on the gate voltage.

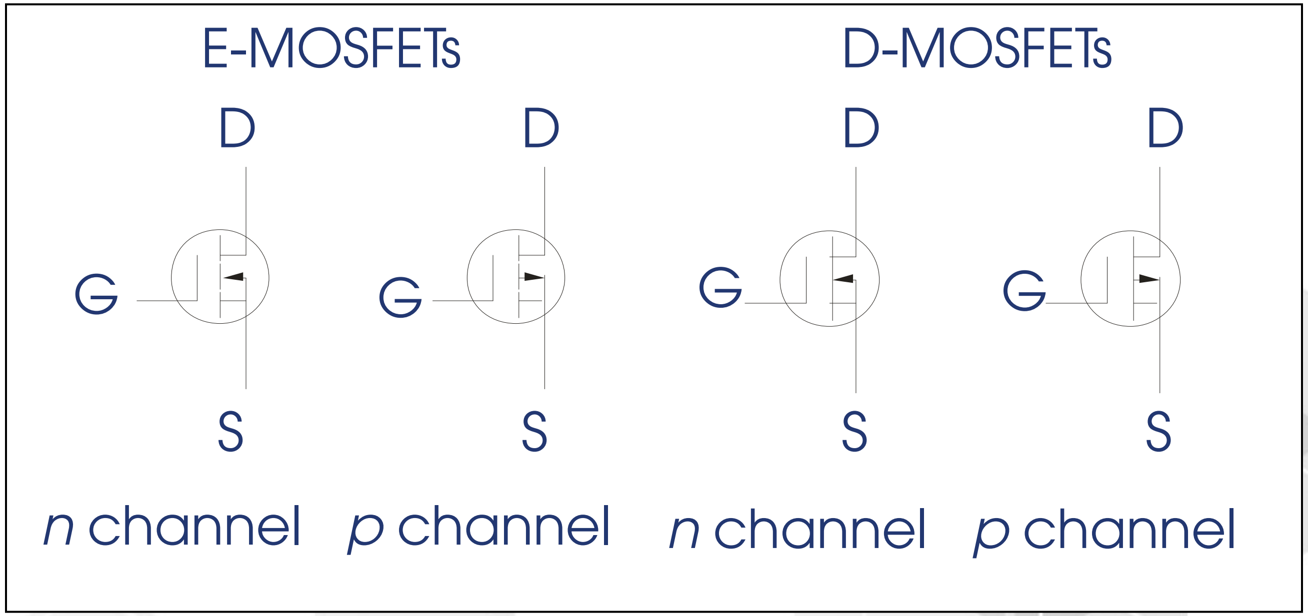
D-MOSFET



operating in D-mode operating in E-mode

The MOSFET

MOSFET symbols are shown. Notice the broken line representing the E-MOSFET that has an induced channel. The *n* channel has an i**n**ward pointing arrow.

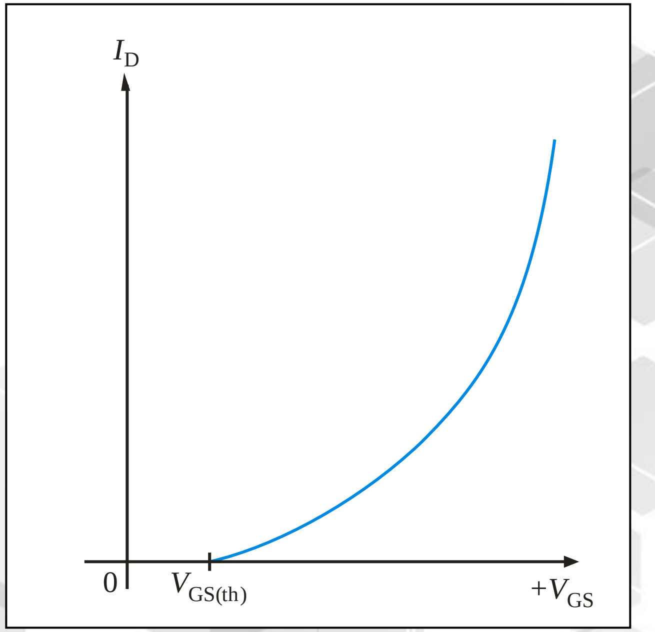


The MOSFET

The transfer curve for a MOSFET is has the same parabolic shape as the JFET but the position is shifted along the *x*-axis. The transfer curve for an *n*-channel E-MOSFET is entirely in the first quadrant as shown.

The curve starts at $V_{GS(th)}$, which is a nonzero voltage that is required to have channel conduction. The equation for the drain current is

$$I_D = K\left(V_{GS} - V_{GS(th)}\right)^2$$



The MOSFET

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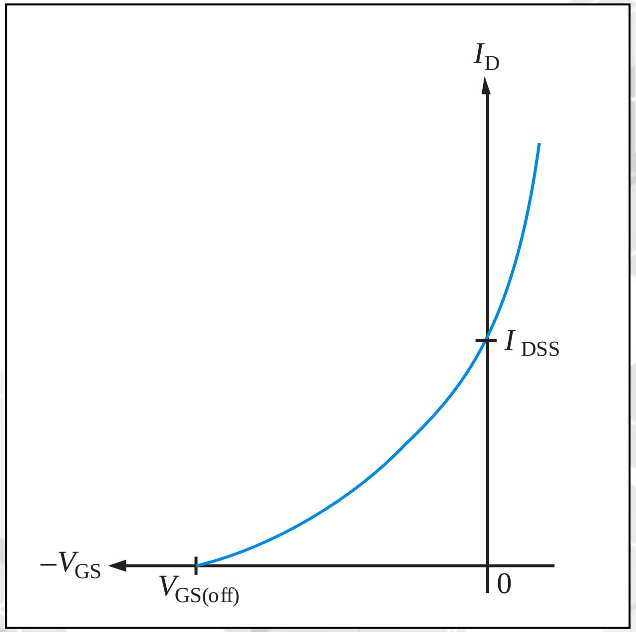
Recall that the D-MOSFET can be operated in either mode. For the *n*-channel device illustrated, operation to the left of the *y*-axis means it is in depletion mode; operation to the right means is in enhancement mode.

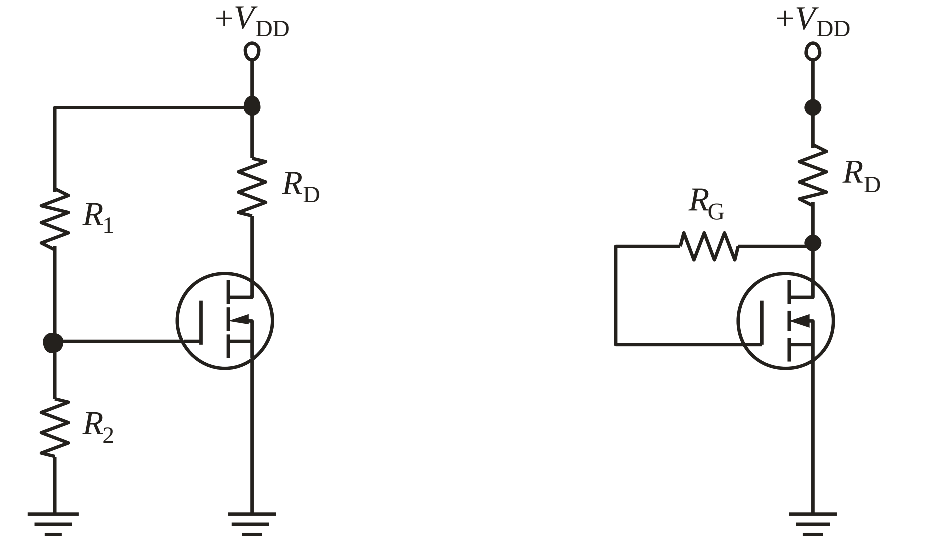
As with the JFET, I_D is zero at $V_{GS(off)}$. When VGS is 0, the drain current is I_{DSS}, which for this device is *not* the maximum current. The equation for drain current is

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$



MOSFET Biasing

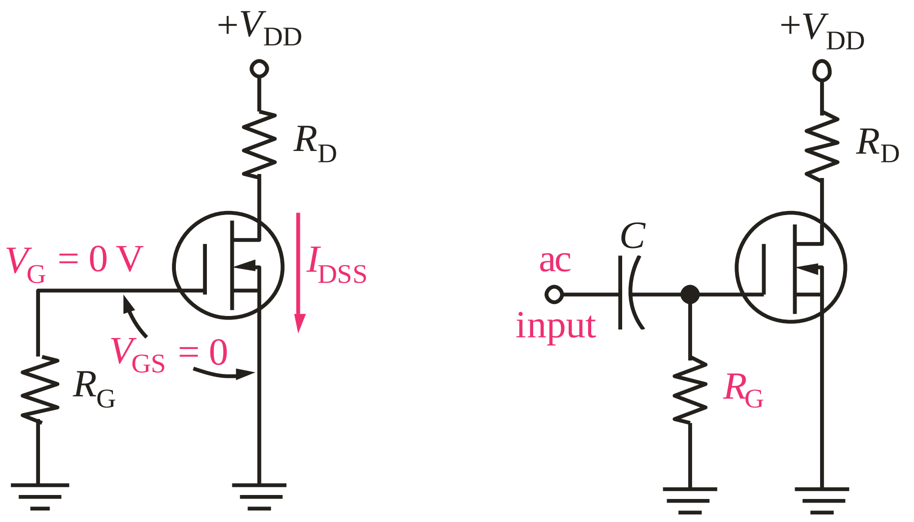
E-MOSFETs can be biased using bias methods like the BJT methods studied earlier. Voltage-divider bias and drain-feedback bias are illustrated for *n*-channel devices.



Voltage-divider bias Drain-feedback bias

MOSFET Biasing

The simplest way to bias a D-MOSFET is with zero bias. This works because the device can operate in either depletion or enhancement mode, so the gate can go above or below 0 V.



Zero bias, which can only be used for the D-MOSFET

FET Amplifiers and Switching Circuits

The Common-Source Amplifier

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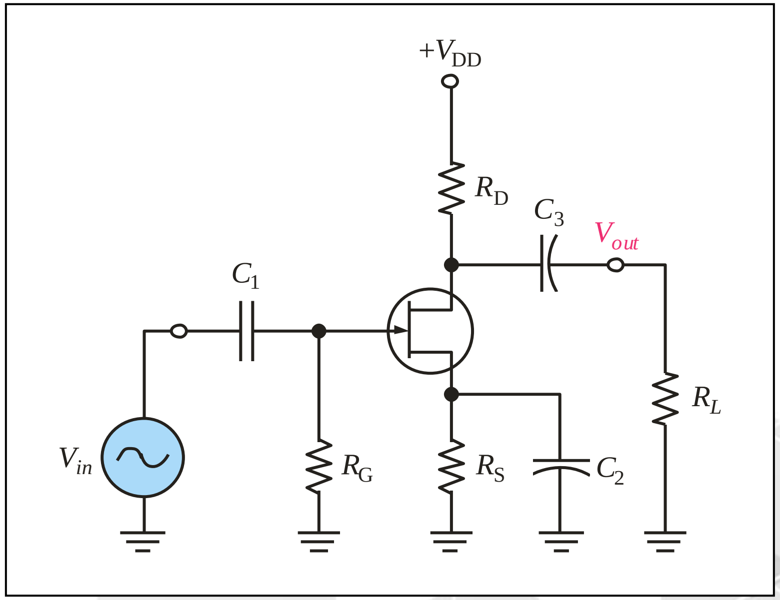
In a CS amplifier, the input signal is applied to the gate and the output signal is taken from the drain. The amplifier has higher input resistance and lower gain than the equivalent CE amplifier.



The voltage gain is given by the equation $A_v = g_m R_d$.

The Common-Source Amplifier

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Recall that conductance is the reciprocal of resistance and admittance is the reciprocal of impedance. Data sheets typically specify the forward transfer admittance, y_{fs} rather than transconductance, g_m. The definition of y_{fs} is

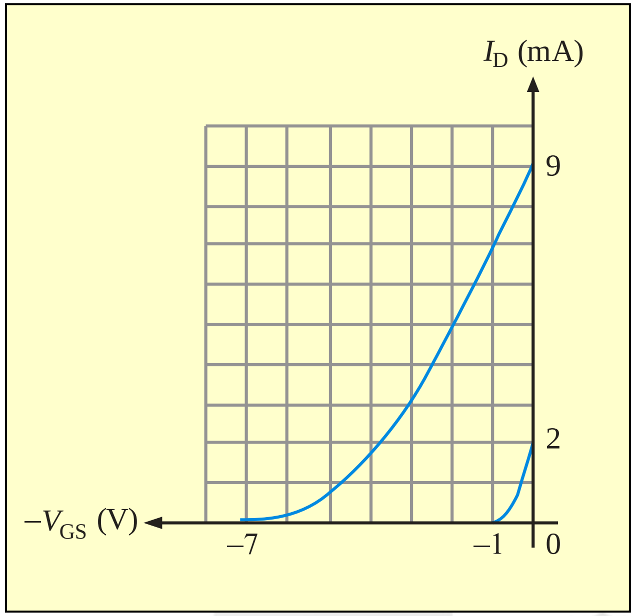
$$y_{fs} = \frac{\Delta I_D}{\Delta V_G}$$

DYNAMIC CHARACTERISTICS		Symbol	Min	Typ	Max	Unit
Forward Transfer Admittance (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457 2N5458	$\lvert Y_{fs} \rvert$	1000 1500	3000 4000	5000 5500	μ mhos

An alternate gain expression for a CS amplifier is $A_v = y_{fs}R_d$.

The Common-Source Amplifier

You can estimate what the transfer characteristic looks like from values on the specification sheet, but keep in mind that large variations are common with JFETs. For example, the range of specified values for a 2N5458 is shown.



OFF CHARACTERISTICS		Symbol	Min	Typ	Max	Unit
Gate-Source Cutoff Voltage (V_{DS} = 15 Vdc, i_D = 10 nAdc)	2N5457 2N5458	$V_{GS(off)}$	-0.5 -1.0	- -	-6.0 -7.0	Vdc

ON CHARACTERISTICS		Symbol	Min	Typ	Max	Unit
Zero Gate-Source Drain Current (V_{DS} = 15 Vdc, V_{GS} = 0)	2N5457 2N5458	I_{DSS}	1.0 2.0	3.0 6.0	5.0 9.0	mAdc

The Common-Source Amplifier

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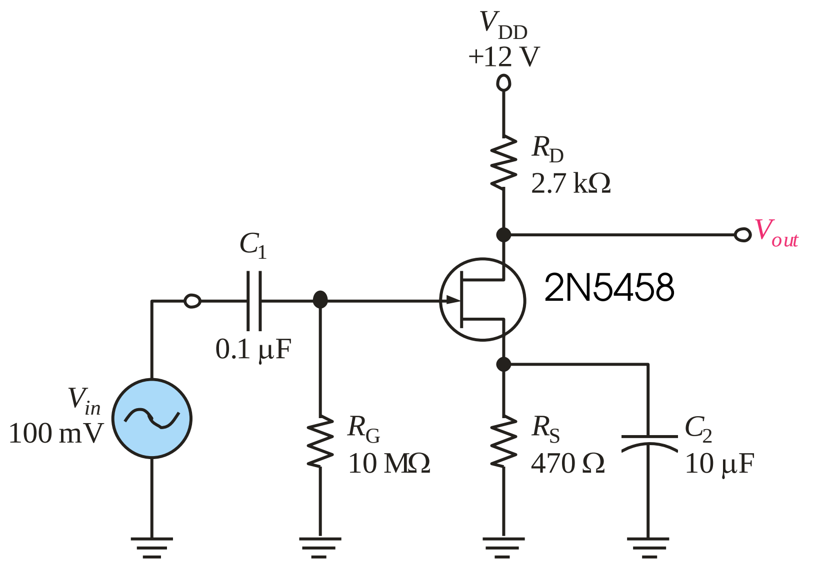
To analyze the CS amplifier. you need to start with dc values. It is useful to estimate I_D based on typical values; specific circuits will vary from this estimate.

Example:

For a typical 2N5458, what is the drain current?

Solution:

From the specification sheet, the typical I_{DSS} = 6.0 mA and $V_{GS(off)}$ = -4 V. These values can be plotted along with the load line to obtain a graphical solution.



See the following slide…

The Common-Source Amplifier

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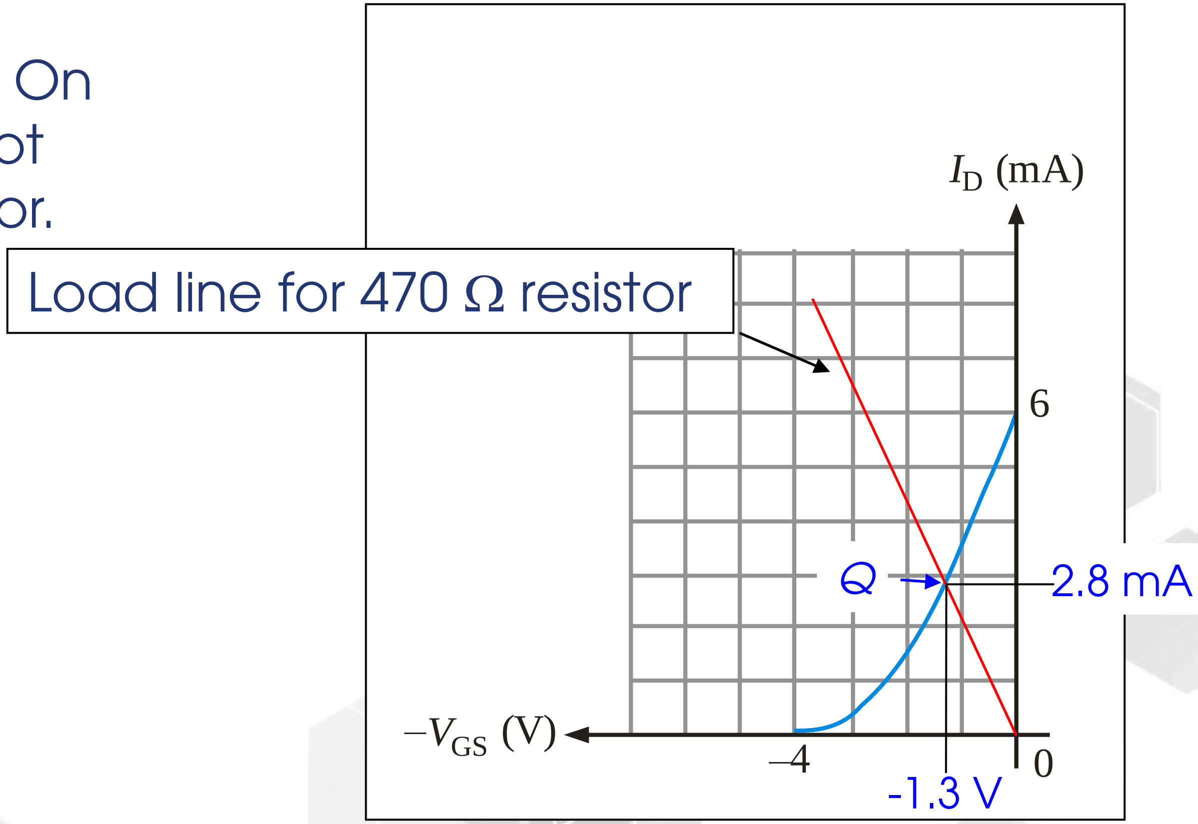
Solution: (continued)

A graphical solution is illustrated. On the transconductance curve, plot the load line for the source resistor.

Then read the current and voltage at the *Q*-point.

I_D = 2.8 mA and V_{GS} = -1.3 V



The Common-Source Amplifier

Solution: (continued)

Alternatively, you can obtain I_D using Equation 9-2: $$I_D = I_{DSS}\left(1 - \frac{I_D R_S}{V_{GS(off)}}\right)^2$$

The solution to this quadratic equation is simplified using a calculator that can handle quadratic equations.

After entering the equation, enter the known values, but leave I_D open. For the typical values for the 2N5458, (I_{DSS} = 6 mA and $V_{GS(off)}$ = -4 V) with a source resistance of 470 Ω, we find 2.75 mA.

```
ID=IDSS∗(1–(–ID∗RS/VG...
  ID= .0027494671581759
  IDSS=.006
  RS= 470
  VGSOFF= 4.0
  bound=(–1E99,1E99)

GRAPH | RANGE | ZOOM | TRACE | SOLVE
```

enter absolute value (for VGSOFF)

press F5

The Common-Source Amplifier

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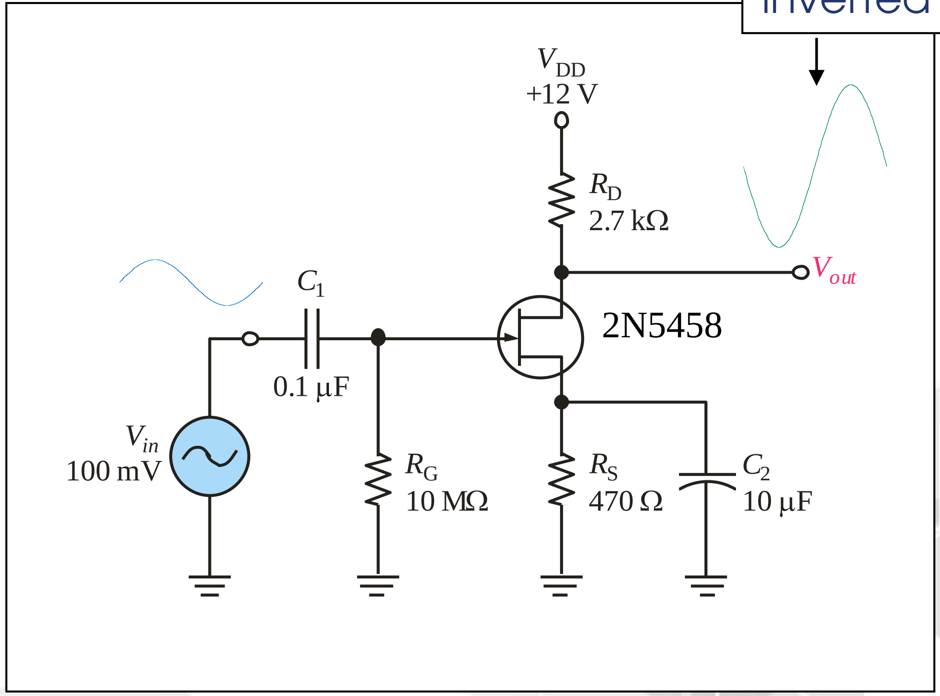
Example: Assume I_{DSS} is 6.0 mA, $V_{GS(off)}$ is -4 V, and V_{GS} = -1.3 V as found previously. What is the expected gain?

Output is inverted



Solution:

$$g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|} = \frac{2(6.0\text{ mA})}{4\text{ V}} = 3.0\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$= 3.0\text{ mS}\left(1 - \frac{-1.3\text{ V}}{-4.0\text{ V}}\right)$$

2.02 mS

$A_v = g_m R_d$ = (2.02 mS)(2.7 kΩ) = 5.45

The Common-Source Amplifier

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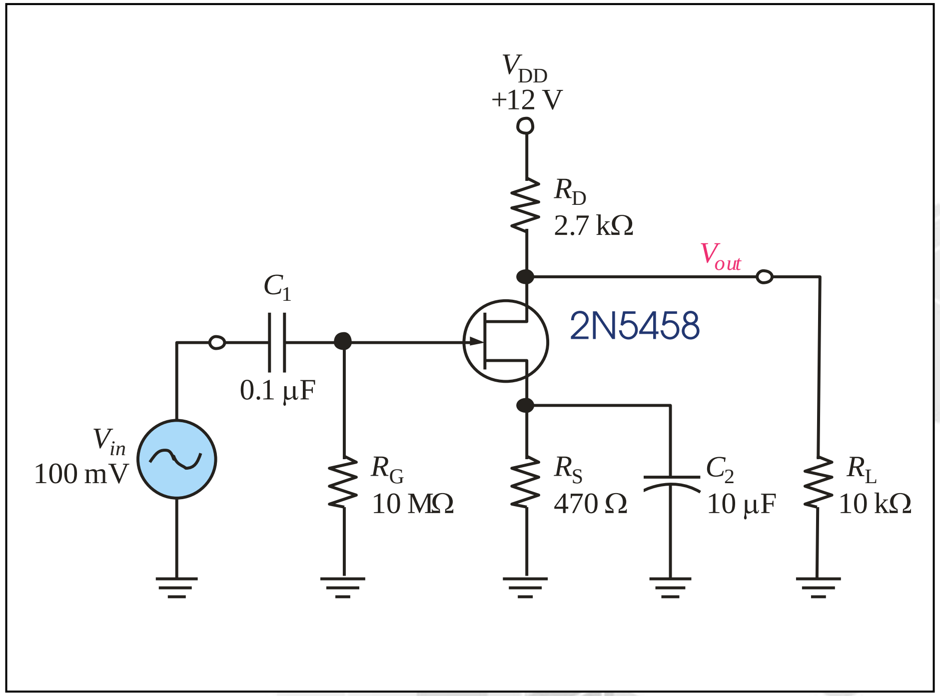
The gain is reduced when a load is connected to the amplifier because the total ac drain resistance (R_d) is reduced.

Example:

How does the addition of the 10 kΩ load affect the gain?



Solution:

$$R_d = \frac{R_D R_L}{R_D + R_L} = \frac{(2.7\ \text{k}\Omega)(10\ \text{k}\Omega)}{2.7\ \text{k}\Omega + 10\ \text{k}\Omega} = 2.13\ \text{k}\Omega$$

$$A_v = g_m R_d = (2.02\ \text{mS})(2.13\ \text{k}\Omega) = 4.29$$

The D-MOSFET

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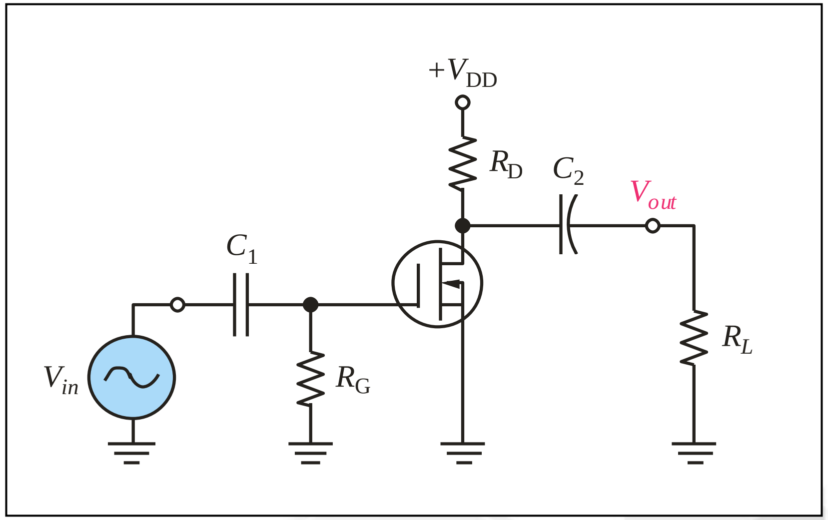
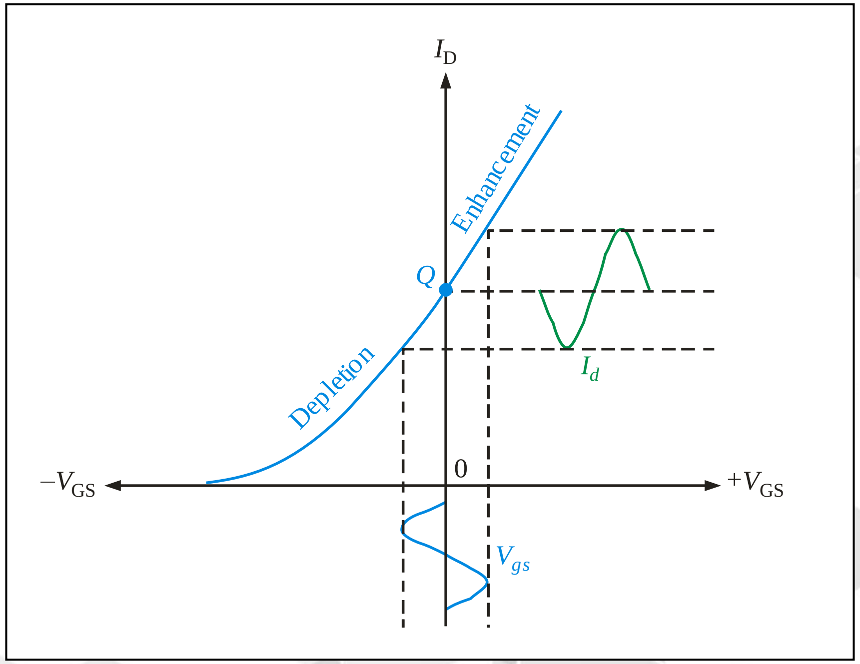
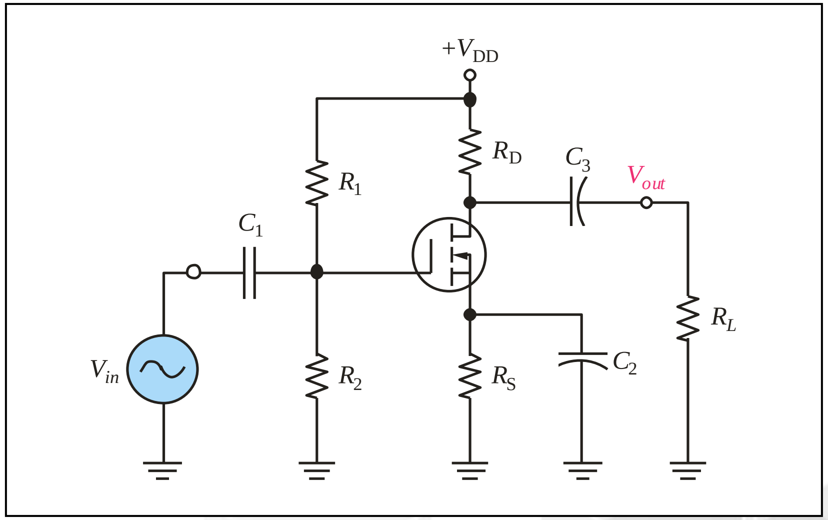
In operation, the D-MOSFET has the unique property in that it can be operated with zero bias, allowing the signal to swing above and below ground. This means that it can operate in either D-mode or E-mode.

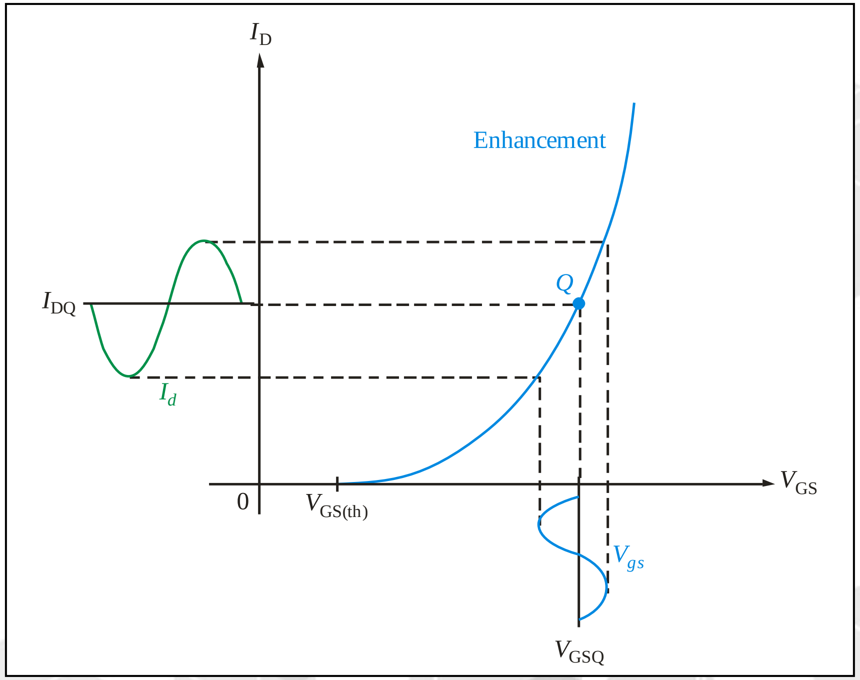




The E-MOSFET

The E-MOSFET is a normally off device. The *n*-channel device is biased on by making the gate positive with respect to the source. A voltage-divider biased E-MOSFET amplifier is shown.





The E-MOSFET

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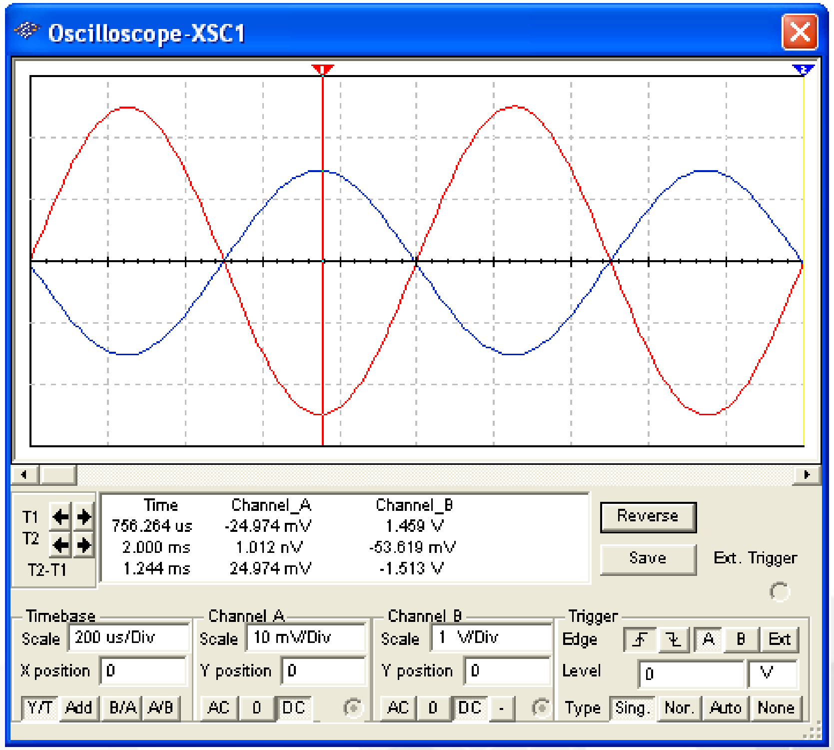
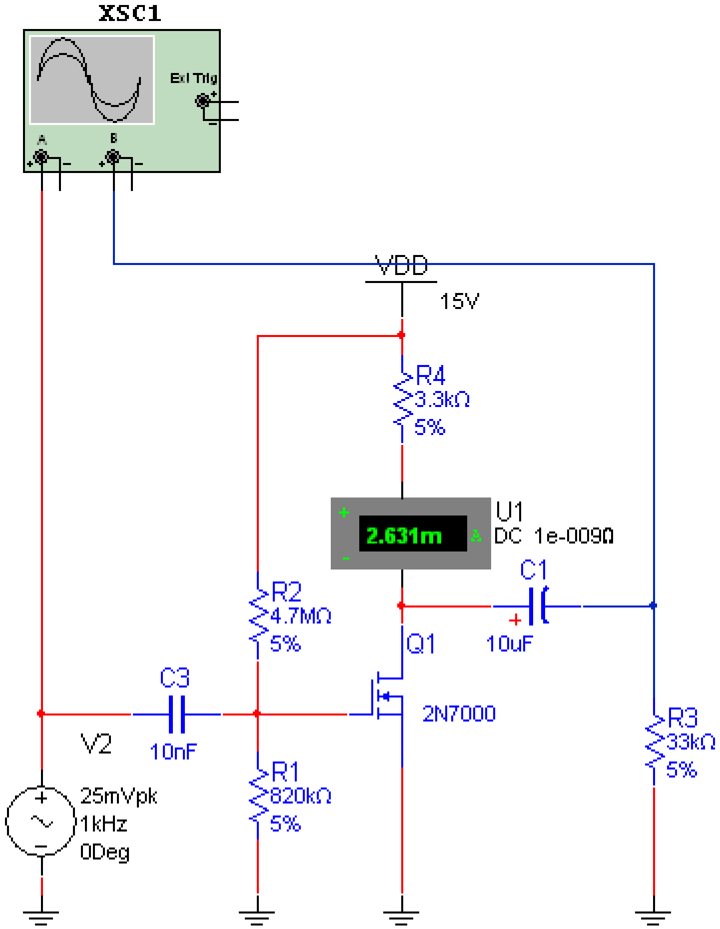
The E-MOSFET amplifier in Example 9-8 is illustrated in Multisim using a 2N7000 MOSFET.





The Common-Drain Amplifier

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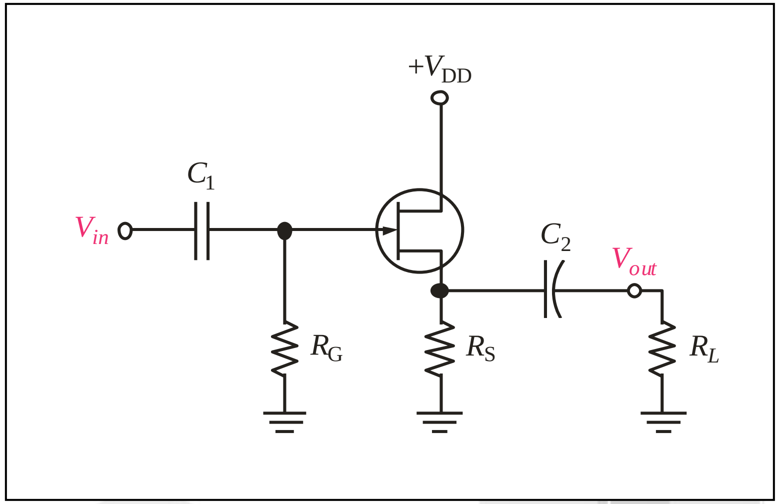
In a CD amplifier, the input signal is applied to the gate and the output signal is taken from the source. There is no drain resistor, because it is *common* to the input and output signals.



The voltage gain is given by the equation $A_v = \frac{g_m R_s}{1 + g_m R_s}$

The voltage gain is always < 1, but the power gain is not.

The Cascode Amplifier

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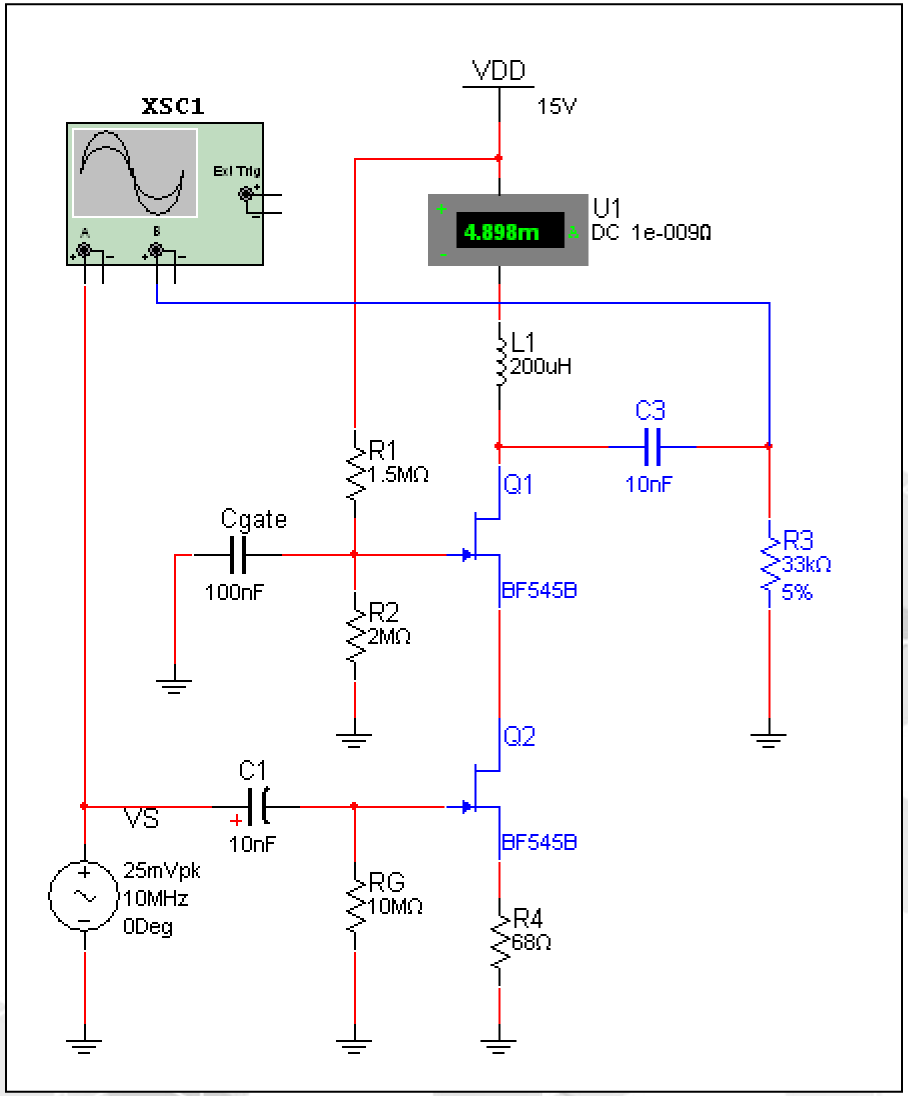
The cascode connection is a combination of CS and CG amplifiers. This forms a good high-frequency amplifier. The input and output signals at 10 MHz are shown for this circuit on the following slide…



The Cascode Amplifier

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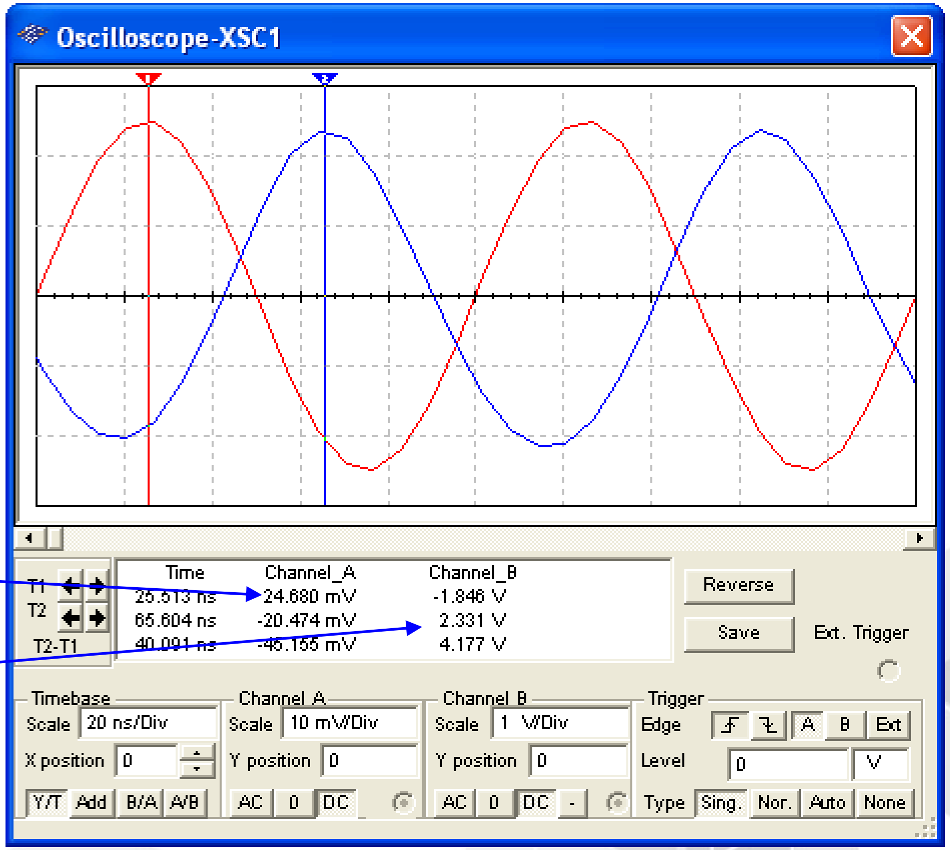
Example:

The input signal for the cascode amplifier is shown in red; the output is blue. What is the gain?



Solution:

The peak of the input is 24.7 mV.

The peak of the output is 2.33 V.

$A_V = 94.3$

The Class-D Amplifier

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MOSFETs are useful as class-D amplifiers, which are very efficient because they operate as switching amplifiers. They use pulse width modulation, a process in which the input signal is converted to a series of pulses. The pulse width varies proportionally to the amplitude of the input signal.

Pulse-width modulation is easy to set up in Multisim. The following slide shows the circuit. A sine wave is compared to a faster triangle wave of the about the same amplitude using a comparator (a 741 op-amp can be used at low frequencies).

The Class-D Amplifier

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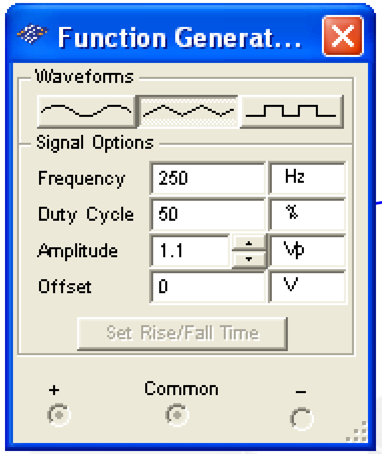
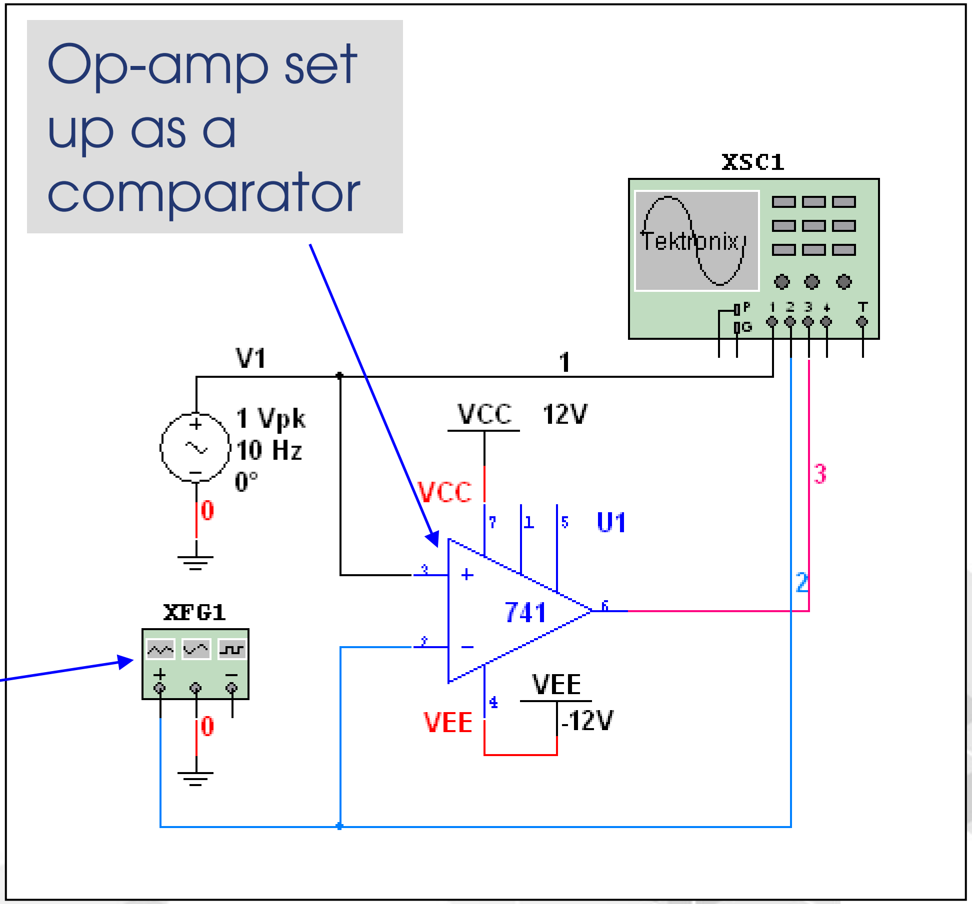
A circuit that you can use in lab or in Multisim to observe pulse width modulation in action. The scope display is shown on the following slide…





The Class-D Amplifier

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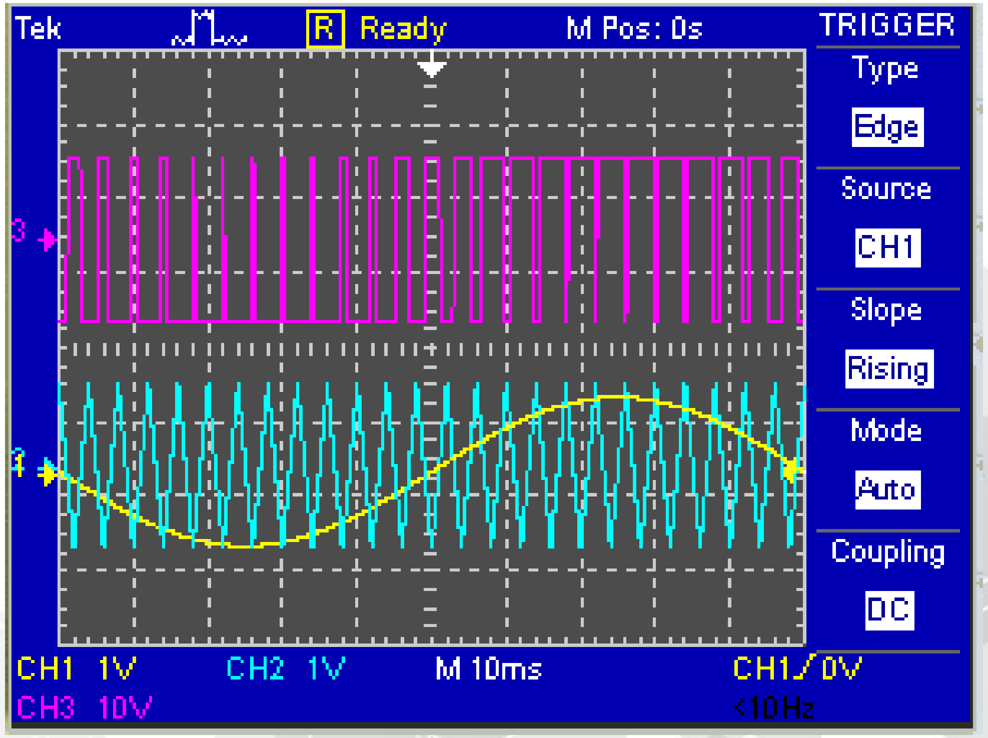
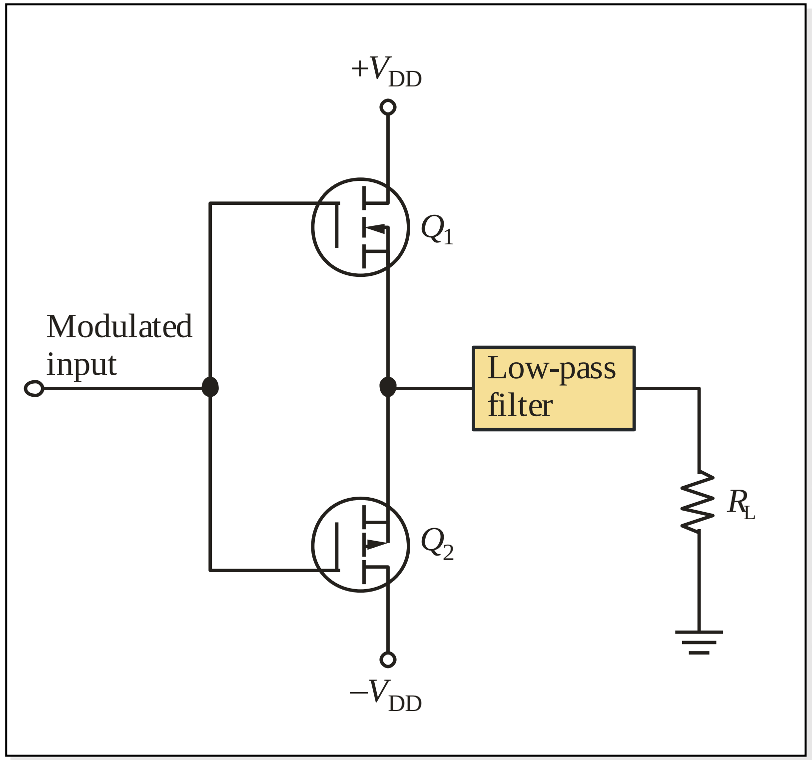
The signal is the yellow sine wave and is compared repeatedly to the triangle (cyan). The result of the comparison is the output (magenta).



The Class-D Amplifier

The modulated signal is amplified by class-B complementary MOSFET transistors. The output is filtered by a low-pass filter to recover the original signal and remove the higher modulation frequency.

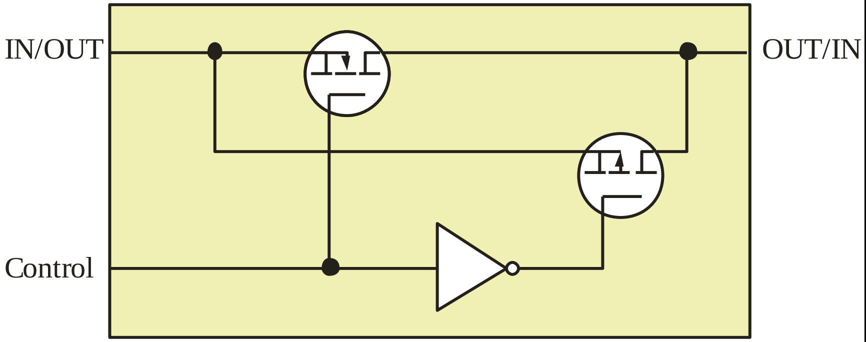
PWM is also useful in control applications such as motor controllers. MOSFETs are widely used in these applications because of fast switching time and low on-state resistance.



The Analog Switch

MOSFETs are also used as analog switches to connect or disconnect an analog signal. Analog switches are available in IC form – for example the CD4066 is a quad analog switch that used parallel *n*- and *p*-channel MOSFETs. The configuration shown allows signals to be passed in either direction.

Advantages of MOSFETs are that they have relatively low on-state resistance and they can be used at high frequencies, such as found in video applications.



Simplified internal construction of a bidirectional IC analog switch.